Features

- Used with the DC004, and DC005 circuits to implement a program control device interface.
- Used with the DC004, DC005, DC006, and DC010 circuits to implement a direct memory access interface.
- Provides two device-interrupt channels.
- Performs a pass-the-pulse interrupt transaction.
- Includes Q-bus drivers and receivers.

Description

The DC003 dual-interrupt circuit, contained in an 18-pin, dual-inline package (DIP), is used in the development of device interfaces for the Q-bus. The simplified logic diagram of the DC003 is shown in Figure 1.

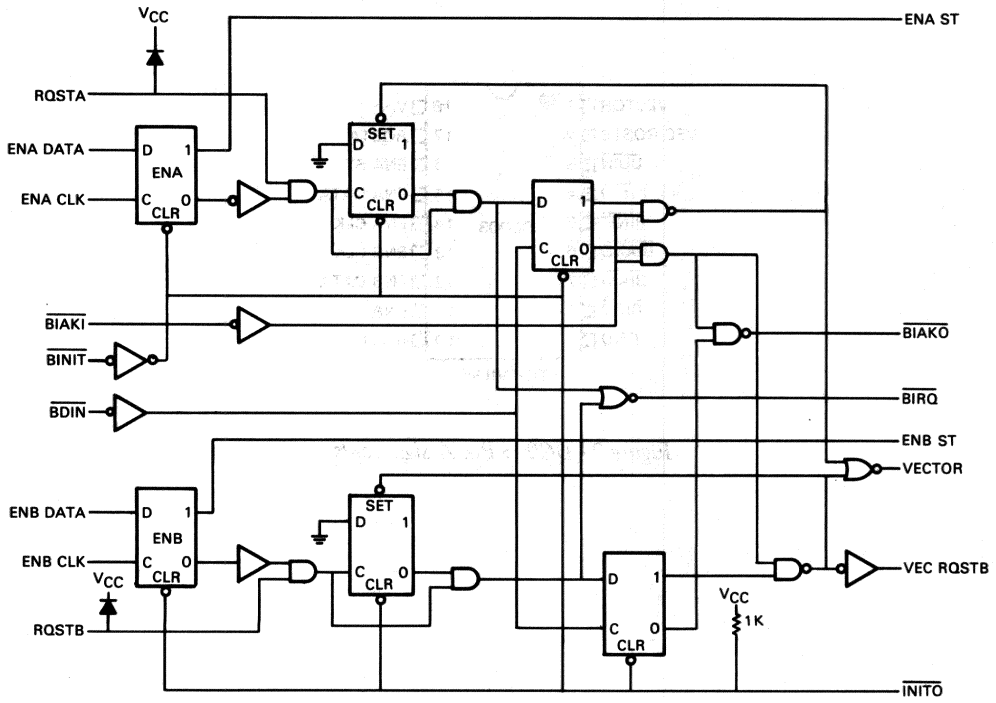

Figure 1 • DC003 Simplified Logic Diagram

It provides the circuits to perform an interrupt transaction in a computer system that uses a daisychain type of arbitration. It includes two interrupt channels; channel A and B, each of which can generate an interrupt request from a device that requires service. The A interrupt logic is assigned a higher priority than the B interrupt logic. Input signals from the bus are received by high-impedance receivers on the DC003 and signals from the DC003 to the bus are supplied by high-current, open-collector driver outputs. The signals levels between the bus and the DC003 are compatible. When a device connected to the interface is not requesting service, the signal from the polling device or processor is passed through the DC003 logic to the next device on the bus. The DC003 circuits includes enable logic and provides interrupt status information to the requesting device.

• Pin and Signal Descriptions

This section provides a brief description of the input and output signals and power and ground connections of the DC003. The pin assignments are identified in Figure 2 and summarized in Table 1.

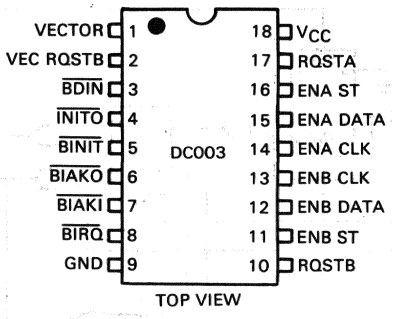

Figure 2 • DC003 Pin Assignments

Table 1 • DC003 Pin and Signal Summary

Pin	Signal	Input/Output	Definition/Function
1	VECTOR	output[1]	Interrupt vector gating—Asserted by the DC003 logic to gate the appropriate vector address onto the bus. This signal forms the bus signal $\overline{\text{BRPLY}}$.
2	VEC RQSTB	output[1]	Vector request B—Asserted by the DC003 logic to indicate that the RQSTB service vector is required and not asserted to indicate that the RQSTA service vector is required. This signal is normally bit 2 of the vector address.
3	$\overline{\text{BDIN}}$	input[2]	Bus data in—Asserted by the master to indicate that an interrupt operation is occurring and always precedes a BIAK signal.
4	$\overline{\text{INITO}}$	output[1]	Initialize out—A buffered $\overline{\text{BINIT}}$ signal from the bus used to initialize the DC003 logic and user device logic
5	$\overline{\text{BINIT}}$	input[2]	Bus initialize—Asserted by the bus to initialize the DC003 logic and device interface logic to a known state.
6	$\overline{\text{BIAKO}}$		Bus interrupt acknowledge output—Asserted by the DC003 logic to pass control to the next device on the bus if the device connected to the DC003 does not require service. Once asserted, it remains passed until the next $\overline{\text{BIAKI}}$ signal is generated.
7	$\overline{\text{BIAKI}}$	input[3]	Bus interrupt acknowledge input—Asserted by the processor in response to the $\overline{\text{BIAKO}}$ signal. The first requesting device prevents the $\overline{\text{BIAKO}}$ signal from being transferred to other devices on the bus and nonrequesting devices will pass the $\overline{\text{BIAKO}}$ signal to the next device. The leading edge of the $\overline{\text{BIAKI}}$ signal clears the $\overline{\text{BIRQ}}$ signal from the DC003.
8	$\overline{\text{BIRQ}}$	output[3]	Bus interrupt request—Asserted by the DC003 logic to indicate that the associated device is requesting an interrupt. This signal is asserted when the RQSTA signal and the ENA DATA signal from the device is asserted. It is cleared when the request signal is removed or on the leading edge of the $\overline{\text{BIAKI}}$ signal after the acceptance of the $\overline{\text{BDIN}}$ signal.
9	GND	input	Ground—Common ground reference
10	RQSTB	input[2]	Device interrupt request B—Asserted by a device requesting an interrupt when the device has asserted the ENB DATA signal. It results in an interrupt request on the $\overline{\text{BIRQ}}$ line that normally remains asserted until the interrupt request is granted.
11	ENB ST	output[1]	Interrupt enable B status—Indicates the status of the interrupt enable B flip-flop on the DC003.

Pin	Signal	Input/Output	Definition/Function
12	ENB DATA	input[1]	Interrupt enable B data—Asserted by a device to enable the transfer of data.
13	ENB CLK	input[1]	A clock pulse from a device that enables the interrupt enable B flip-flop to assume the state of the ENB DATA signal.
14	ENA CLK	input[1]	A clock pulse from a device that enables the interrupt enable A flip-flop to assume the state of the ENA DATA signal.
15	ENA DATA	input[1]	Interrupt enable A data—Asserted by a device to enable the transfer of data.
16	ENA ST	output[1]	Interrupt enable A status—Indicates the status of the interrupt enable A flip-flop on the DC003.
17	RQSTA	input[2]	Device interrupt request A—Asserted by a device requesting an interrupt when the device has asserted the ENA DATA signal. It results in an interrupt request on the $\overline{\text{BIRQ}}$ line that normally remains asserted until the interrupt request is granted.
18	V_{CC}	input	Voltage—Power supply dc voltage

[1]TTL level
[2]high-impedance
[3]open-collector

• Application Information

Refer to the *Chipkit Users Manual LSI-11 Bus Interface Chips* (document no. EJ-01387-92) for general application information. The Q-bus is an LSI-11 bus.

• Specifications

The mechanical, electrical, and environmental characteristics and specifications for the DC003 are described in the following paragraphs. The test conditions for the electrical values are as follows unless specified otherwise.

- Operating temperature (T_A): 0°C to 70°C
- Supply voltage (V_{CC}): 5.0 V ±5%

Mechanical Configuration

The physical dimensions of the DC003 18-pin DIP package are contained in Appendix E. The materials and construction of the molded DIP are defined in Digital Specification A-PS-1900002-GS.

Absolute Maximum Ratings

Stresses greater than the absolute maximum ratings may cause permanent damage to the device. Exposure to the absolute maximum ratings for extended periods may adversely affect the reliability of the device.

- Supply voltage (V_{CC}): 7.0 V
- Input voltage (V_I): 5.5 V
- Operating temperature (T_A): 0°C to 70°C
- Storage temperature (T_S): −65°C to 150°C

Recommended Operating Conditions

- Supply voltage (V_{CC}): 4.75 V (minimum), 5.0 V (normal), 5.25 V (maximum)
- Supply current (I_{CC}): 140 mA (maximum)
- Free-air temperature: 0°C to 70°C
- Relative humidity: 10% to 95% (noncondensing)

dc Electrical Characteristics

The dc electrical characteristics of the DC003 for the operating voltage and temperature ranges specified are listed in Tables 2 through 4. Table 2 lists the dc specifications of the TTL input and output circuits that do not connect to the bus. Table 3 lists the dc specifications for the high-impedance receivers that connect to the LSI-11 bus. Table 4 lists the dc specifications for the open-collector driver outputs that connect to the bus. Refer to Appendix C for the test circuit configurations referenced in the tables.

Table 2 • DC003 TTL Input and Output Parameters (nonbus)

Parameter	Symbol	Test Condition	Requirements Min.	Requirements Max.	Units	Test Circuit
High-level input voltage	V_{IH}		2.0	—	V	C1, C2
Low-level input voltage	V_{IL}		—	0.8	V	C1, C2
Input clamp voltage	V_I	V_{CC} = 4.75 V I_I = −18 mA	—	−1.2	V	C3
High-level output voltage	V_{OH}	V_{CC} = 4.7 V I_O = −1.0 mA	2.7	—	V	C1
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V I_O = 20 mA	—	0.5	V	C2
Input current at maximum input voltage	I_I	V_{CC} = 5.25 V V_I = 5.5 V	—	1.0	mA	C4
High-level input current	I_{IH}	V_{CC} = 5.25 V V_I = 2.7 V[1]	—	50	μA	C4

Parameter	Symbol	Test Condition	Requirements Min.	Max.	Units	Test Circuit
Low-level input current	I_{IL}	V_{CC}=5.25 V V_I=0.5 V[2]	—	-0.55	mA	C5
Short-circuit output current	I_{OS}	V_{CC}=5.25 V[3]	-40	-100	mA	C6
Supply current	I_{CC}	V_{CC}=5.25 V	—	140	mA	C7

[1]I_{IH} = 100 µA at pins 12 and 15.
[2]I_{IL}–2.0 mA at pins 12 and 15.
[3]Not more than one output shall be short circuited at a time and the duration of the short must not exceed 1 second.
[4]Does not apply to pin 4.

Table 3 • DC003 High-impedance Bus Receiver Parameters

Parameter	Symbol	Test Condition	Requirements Min.	Max.	Units	Test Circuit
High-level input voltage	V_{IH}	V_{CC}=4.75 V	1.53	—	V	C1,C2
	V_{IH}	V_{CC}=5.25 V	1.70	—	V	C1,C2
Low-level input voltage	V_{IL}	V_{CC}=4.75 V	—	1.30	V	C1,C2
	V_{IL}	V_{CC}=5.25 V	—	1.47	V	C1,C2
Input clamp voltage	V_I	V_{CC}=4.75 V I_I=-18 mA	—	-1.2	V	C3
	V_I	V_{CC}=4.75 V I_I=18 mA[1]	—	6.25	V	C3
High-level input current	I_{IH}	V_{CC}=0 V V_I=3.8 V[2]	—	40	µA	C4
	I_{IH}	V_{CC}=5.25 V	—	40	µA	C4
Low-level input current	I_{IL}	V_{CC}=0 V V_I=0.5 V[2]	—	-10	µA	C5
	I_{IL}	V_{CC}=5.25 V	—	-10	µA	C5

[1]Pins 10 and 17 only.
[2]Exclude pins 10 and 17.

Table 4 • DC003 Open-collector Bus Driver Parameters

Parameter	Symbol	Test Condition	Requirements Min.	Max.	Units	Test Circuit
Output reverse current	I_{OR}	$V_{CC}=4.75$ V $V_{OH}=3.5$ V	—	25	μA	C1
Low-level output voltage	V_{OL}	$V_{CC}=4.75$ V $I_{sink}=70$ mA	—	0.8	V	C2
		$V_{CC}=4.7$ V $I_{sink}=16$ mA	—	0.5	V	C2

ac Electrical Characteristics

The input/output signal timing for the interrupt logic A is shown in Figure 3. The input/output signal timing for interrupt logic A and interrupt logic B is shown in Figure 4. Refer to Appendix D for the standard input voltage waveforms and for the signal propagation delay measurements. The load circuit configurations used in measuring the TTL outputs and open-collector outputs are shown in Figure 5.

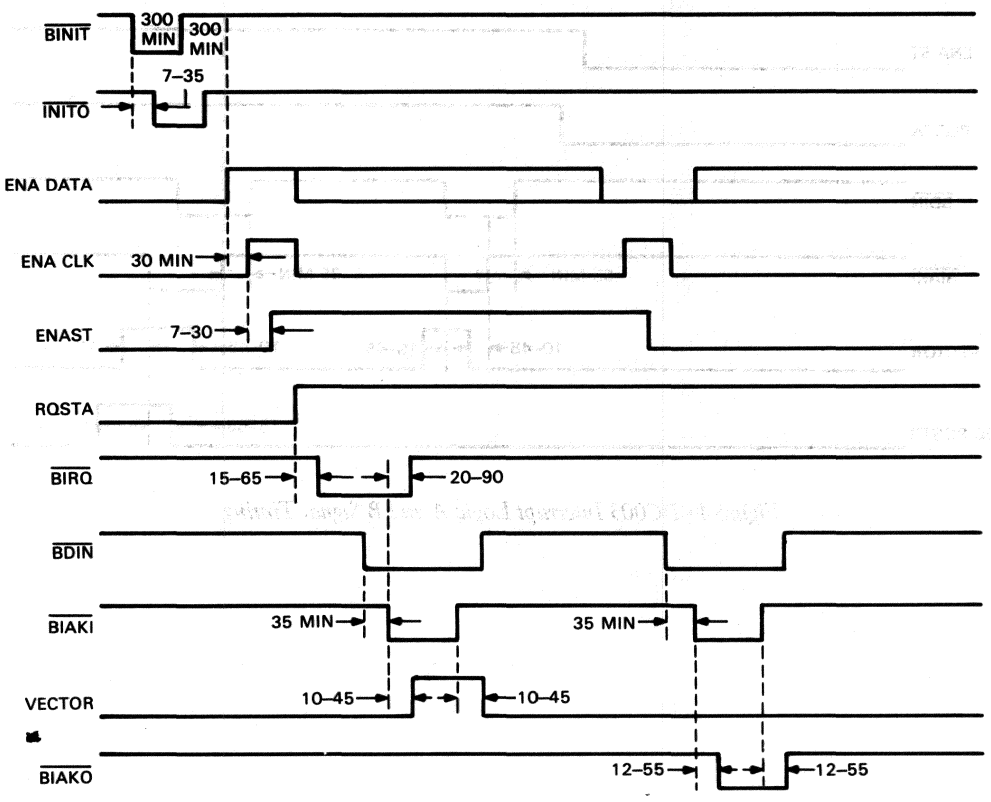

Figure 3 • DC003 Interrupt Logic A Signal Timing

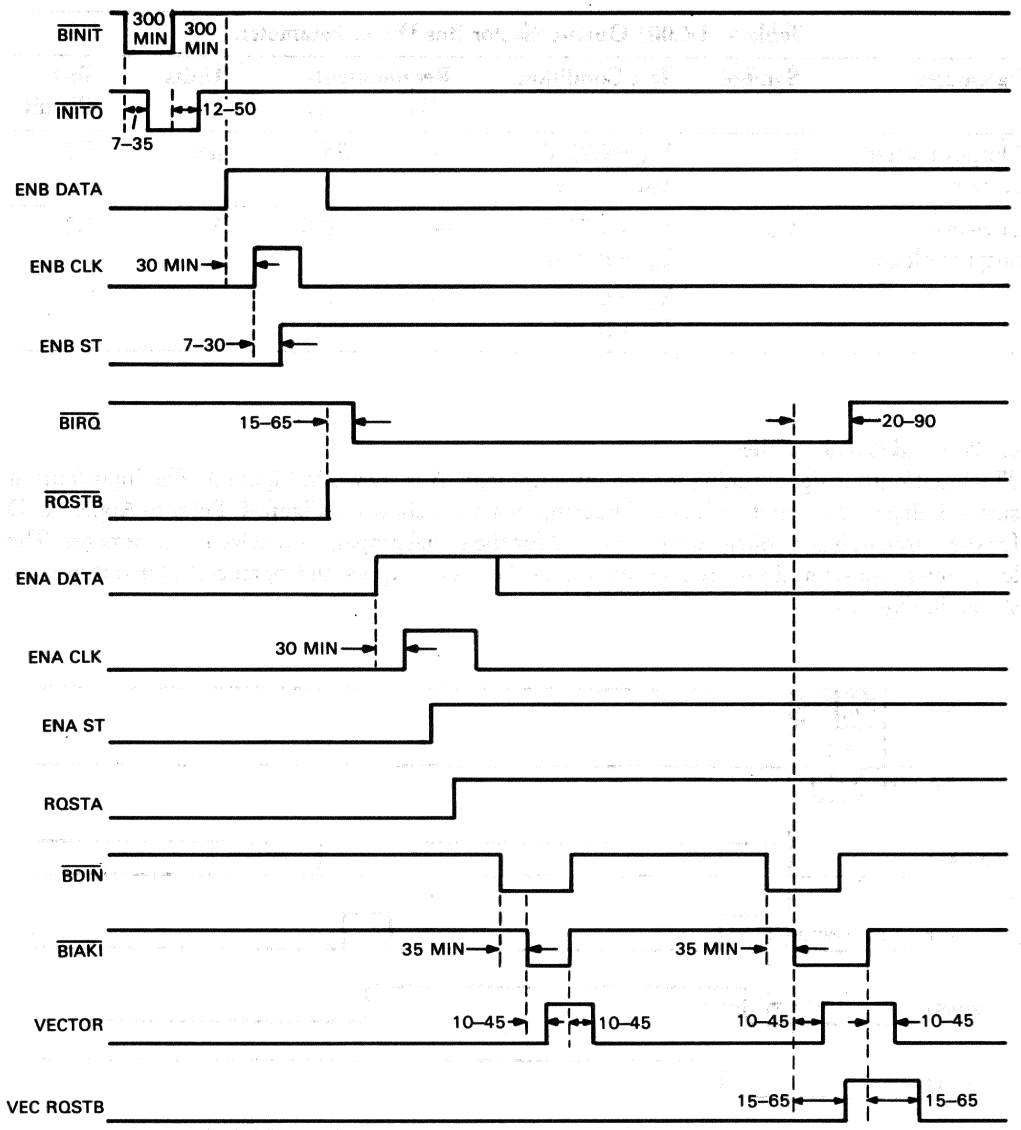

Figure 4 ▪ DC003 Interrupt Logic A and B Signal Timing

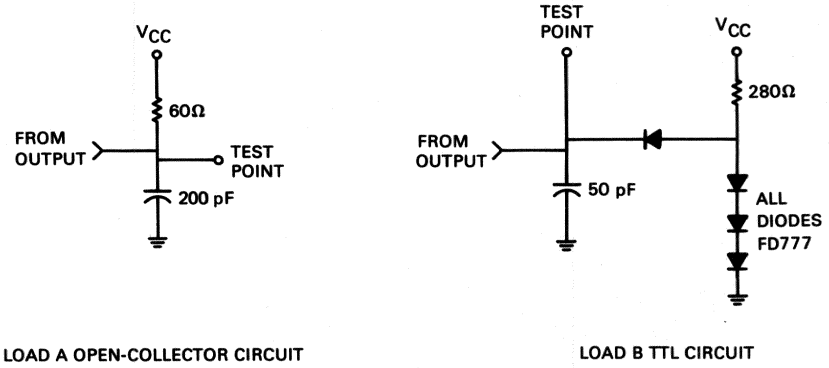

Figure 5 • DC003 Output Load Circuits